IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellants:	Richard Kessler et al.	§ §	Confirmation No.:	8193
Serial No.:	10/677,583	§ §	Group Art Unit:	2182
Filed:	October 2, 2003	§ §	Examiner:	A. Hassan
For:	Scalable Efficient I/O Port Protocol	§ §	Docket No.:	200301779-2

APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Date: June 9, 2009

Sir:

Appellants hereby reinstate the appeal of this matter, and submit this Appeal Brief in response to the Office action dated March 18, 2009. A Notice of Appeal was filed December 9, 2008, and both the Notice of Appeal Fee and Appeal Brief Fee have already been paid.

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I. REAL PARTY IN INTEREST

The real party in interest is the Hewlett-Packard Development Company (HPDC), a Texas Limited Partnership, having its principal place of business in Houston, Texas. HPDC is a wholly owned affiliate of Hewlett-Packard Company (HPC). HPC merged with Compaq Computer Corporation (CCC) which owned Compaq Information Technologies Group, L.P. (CITG). In the parent case, Serial No. 09/652,391 (now U.S. Pat. No. 6,738,836), the Assignment from the inventors to CCC was recorded on 08/31/2000, at Reel/Frame 011142/0283. The Assignment from CCC to CITG was recorded on 01/15/2002, at Reel/Frame 012470/0938. The Change of Name document was recorded on 12/02/2003, at Reel/Frame 014177/0428. In the present case, the Change of Name document was recorded on 05/12/2004 at Reel/Frame 014628/0103.

II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related appeals or interferences.

III. STATUS OF THE CLAIMS

Originally filed claims: 1-9.

Added claims: 10-16.

Claim cancellations: 1-2, 5-16.

Presently pending claims: 3 and 4.

Presently appealed claims: 3 and 4.

IV. STATUS OF THE AMENDMENTS

No claims were amended after the final Office action dated March 18, 2009.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

The various embodiments are directed to a scalable efficient input/output (I/O) port protocol. **{Specification Title}.** At least some of the illustrative embodiments are those as defined in claim 3:

> 3. A distributed multiprocessing computer system, comprising:
>
> a plurality of processors each coupled to an I/O bridge; **{Specification Page 8, lines 1-5; Figure 1, elements 100 and 104}**
>
> a plurality of memory modules coupled one each to the plurality of processors **{Specification Page 8, lines 1-5; Page 8, lines 19-23; Figure 1, element 102}**, each memory module able to store data blocks that are shared between said processors **{Specification Page 9, lines 1-3}**, wherein coherence of the shared data blocks is maintained using a directory based coherence protocol; **{Specification Page 6, lines 8-10; Page 20, lines 18-22}**[1]
>
> at least one I/O device coupled to the I/O bridge **{Specification Page 8, lines 15-18; Figure 1, elements 105 and 106}**, the I/O device and I/O bridge performs direct memory access (DMA) to transfer data blocks to the memory modules; **{Specification Page 22, lines 11-14}** and
>
> wherein the I/O bridge obtains exclusive ownership of shared memory module data blocks during I/O device access **{Specification Page 22, line 19 – Page 23, line 9; Page 25, lines 4-6}**, and wherein said I/O bridge includes a DMA device configured to perform both in-order and out-of-order DMA reads and writes on streams of data blocks. **{Out-of-order– Specification Page 23, lines 17 – 27; In-order– Page 24, lines 1-12}**

Yet still other illustrative embodiments are those as defined in claim 4:

> 4. The distributed multiprocessing computer system of claim 3 wherein the DMA device that performs an in-order stream of reads of data blocks always receives coherent data blocks that do not have to be written back to the memory module. **{Specification Page 6, lines 14-18; Page 24, line 17 – Page 25, line 3}**

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[1] "The front-end DIFT 191 performs a number of functions such as managing the processor's directory-based memory coherency... ." **{Specification Page 6, lines 8-10; Page 20, lines 18-22}.**

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 3 and 4 are obvious under 35 USC § 103(a) over Sharma et al. (U.S. Patent No. 6,647,469, hereafter "Sharma") and Bertone et al. (U.S. Patent No. 5,522,069, hereafter "Bertone").

VII. ARGUMENT

A. Section 103 Rejections of Claims 3 and 4 over Sharma and Bertone

1. Claim 3

Claim 3 stands rejected as allegedly obvious over Sharma and Bertone.

Claim 3 specifically recites, "wherein said I/O bridge includes a DMA device that supports both in-order and out-of-order DMA read and write streams of data blocks." The Office action admits Sharma fails to disclose at least the out-of-order structure.[2] The Office action attempts to rely on Bertone's Col. 17, lines 13-23;[3] however, the reliance is misplaced.

Bertone is directed to a symmetric multiprocessing system with unified environment and distributed system functions.[4] Bertone's Figure 1 (comprising 1A and 1B) is reproduced below for convenience of the discussion.

Fig. 1A

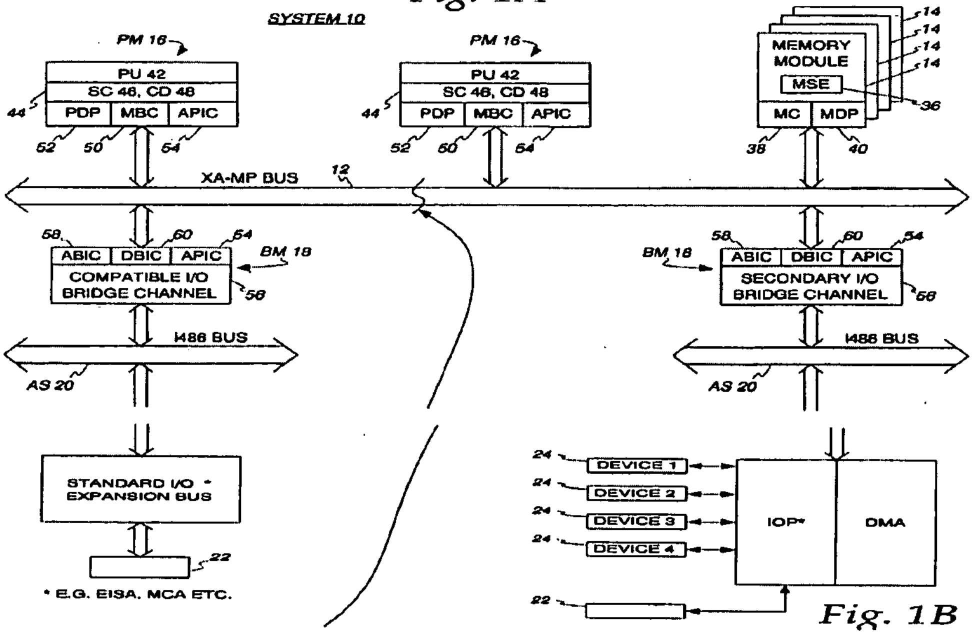

Fig. 1B

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[2] Office action of March 18, 2009, Page 3, second paragraph.

[3] Office action of March 18, 2009, page 3, third paragraph.

[4] Bertone Title.

In particular, Bertone appears to describe a symmetric multiprocessor system having as a backbone an extended architecture multiple processor (XA-MP) bus 12.[5] Devices expressly directly coupled to the XA-MP bus 12 include memory modules (MM) 14, processor modules (PM) 16 and bridge modules (BM) 18.[6] Devices directly connected to the XA-MP bus 12 appear to be able to implement both in-order data transfer, and out-of-order data transfer across the XA-MP bus 12.[7] However, input/output (I/O) devices 24, and their associated DMA controller (lower right of figure), do not appear to couple directly to the XA-MP bus 12.

I/O devices 24 couple to the Bertone system through the BM 18 and AS bus 20.[8] DMA for I/O devices appears to be handled by DMA controllers in devices coupled downstream of the AS bus 20, not the BM 18.

> It is also contemplated that associated with the AS bus there will typically be standard PC support hardware, such as an interrupt controller, several direct memory access devices ... that permits accessory devices to gain access to and control of the AS bus 20. Most typically, direct memory access devices carrying out such task as disk reads and writes will, in response to command received from the central processing units, set up direct memory access (DMA) reads and writes to and from the disk drives over the EISA or MCA bus controller... .
>
> With respect to FIG. 9, functionality the bridge interface controller presents a XA-MP bus window to the AS bus 20 through which DMA controllers ... can address data store and retrieval commands in precisely the same manner as if these commands were directed to the RAM memory associated with conventional i486 microprocessor.[9]

Thus, Bertone does not appear to teach out-of-order DMA for I/O device accesses. Stated otherwise, while devices directly coupled to Bertone's XA-MP bus 12 (like the BM 18) may perform non-DMA transactions out-of-order, the out-of-order processing of Bertone does not appear to extend to the I/O device DMA accesses of Bertone. Moreover, even if Bertone's BM 18 is considered to the claimed I/O bridge (which Appellants do not admit), the DMA controllers of Bertone do not appear to be in the BM 18. Thus, even if the teachings of Sharma are precisely as the Office action suggests (which Appellants do not admit), Sharma and Bertone still fail to teach "said I/O bridge includes a DMA device that supports both in-order and out-of-order DMA read and write streams of data blocks."

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[5] Bertone Col. 2, lines 65-68.

[6] Bertone Col. 3, lines 1-8.

[7] Bertone Col. 3, lines 43-53.

[8] Bertone Col. 3, lines 10-16; Col. 24, lines 54-64.

[9] Bertone Col. 24, line 65 through Col. 25, line 16.

Based on the foregoing, Appellants respectfully submit that the rejection of the claim be reversed, and the claim set for issue.

2. Claim 4

Claim 4 stands rejected as allegedly anticipated by Sharma.

Claim 4 specifically recites, "wherein the DMA device that performs an in-order stream of reads of data blocks always receives coherent data blocks that do not have to be written back to the memory module." The portion of Sharma relied upon by the final Office action, Sharma's Col. 9, lines 30-67, is directed to the content of a DMA request. A DMA request may be used for many request types.[10] With respect to reads, the cited section states:

> If another I/O bus (145 of FIG. 4) had made a previous request for the specific cache line, the I/O bus currently requesting the data may also be allowed access to the data if the ownership is not read current and the cache line is valid.[11]

Clearly Sharma contemplates several different read access situations, and thus Appellants respectfully submit that Sharma and Bertone fail to teach or fairly suggest "wherein the DMA device that performs an in-order stream of reads of data blocks **always** receives coherent data blocks that do not have to be written back to the memory module."

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[10] For example, block 520 identifies the request type as read or write. Sharma Col. 9, lines 57-59.

[11] Sharma, Col. 9, lines 42-46.

Based on the forgoing, Appellants respectfully submit that the rejection of claim 4 be reversed, and the claim set for issue.

B. Conclusion

For the reasons stated above, Appellants respectfully submit that the Examiner erred in rejecting all pending claims. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,

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Mark E. Scott
PTO Reg. No. 43,100
CONLEY ROSE, P.C.
(512) 610-3410 (Phone)
(512) 610-3456 (Fax)
ATTORNEY FOR APPELLANTS

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
Legal Dept., M/S 35
P.O. Box 272400
Fort Collins, CO 80527-2400

VIII. CLAIMS APPENDIX

1.–2. (Cancelled).

3. (Previously presented) A distributed multiprocessing computer system, comprising:

a plurality of processors each coupled to an I/O bridge;

a plurality of memory modules coupled one each to the plurality of processors, each memory module able to store data blocks that are shared between said processors, wherein coherence of the shared data blocks is maintained using a directory based coherence protocol;

at least one I/O device coupled to the I/O bridge, the I/O device and I/O bridge performs direct memory access (DMA) to transfer data blocks to the memory modules; and

wherein the I/O bridge obtains exclusive ownership of shared memory module data blocks during I/O device access, and wherein said I/O bridge includes a DMA device configured to perform both in-order and out-of-order DMA reads and writes on streams of data blocks.

4. (Original) The distributed multiprocessing computer system of claim 3 wherein the DMA device that performs an in-order stream of reads of data blocks always receives coherent data blocks that do not have to be written back to the memory module.

5.-16. (Cancelled).

IX. EVIDENCE APPENDIX

None.

X. RELATED PROCEEDINGS APPENDIX

None.